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Tiempo Unveils First Timing-Driven Design Flow for its Innovative Clockless Chip Design Technology

Support for standard SDC format by Tiempo's ACC tool enables design of fast asynchronous circuits with low-power

Grenoble, France – June 07, 2010 – Tiempo,SAS, a developer of innovative clockless technology for the design of low power integrated circuits (ICs), today announced its ability to support the use of its asynchronous IP blocks with a true timing-driven design methodology using standard SDC formats. Designers can now characterize and constrain clockless blocks in order to ensure a targeted performance. This milestone further establishes asynchronous design as a viable option for achieving low power and other critical design objectives.

At a demonstration at the 47th annual Design Automation Conference, Tiempo will show that its asynchronous technology is compatible with timing constraints used by popular EDA tools and synchronous design styles. Using a sample asynchronous IP block from Tiempo's library of delay-insensitive designs, the flow consists of the compilation of an asynchronous block with its synchronous interfaces having a SDC constraint file attached.

The Tiempo Asynchronous Circuit Compiler (ACC) synthesis tool then generates a netlist and outputs new design constraints for hand off to the timing-driven flow. In Tiempo's demonstration at DAC, the outputs from the Tiempo tool are sent to Synopsys' IC Compiler™ place-and-route solution to drive a timing driven place and route process. A timing check can be performed using Synopsys' PrimeTime™ timing signoff tool.

The integration allows designers to be sure that no timing violations arise from the use of Tiempo's asynchronous technology, and that the performance requirements expected of the company's IP are met.

"The successful integration of our asynchronous technology with standard EDA flows will help further accelerate the adoption of clockless technology and open the door for a wide variety of applications that need the low power and high performance benefits asynchronous styles enable," said Alban d'Halluin, Director Product Marketing at Tiempo. "Meeting timing objectives is critical in all types of IC design, and now for the first time designers can apply asynchronous design techniques without worrying about their impact on chip-level timing issues."

Tiempo's asynchronous circuits are fully clock-less and self-controlled and their behavior is governed by signal transitions rendezvous and signal level memorization. These principles, implemented with Tiempo's efficient and intuitive coding style, ensure functional correctness regardless of any actual delay through gates and wires.

Tiempo's SystemVerilog-based asynchronous coding style offers designers a very simple and efficient way to write high-level models of asynchronous designs that are automatically synthesized with ACC into a Verilog gate-level netlist. SystemVerilog asynchronous models can be written by designers who are not expert in asynchronous design, and most of the implementations details of Tiempo unique asynchronous design technology are hidden to the designer.

At the 47th DAC, Tiempo will demonstrate in its booth # 710:

- A timing-driven flow for integrating an asynchronous IP block into a synchronous system. From a SystemVerilog source file with SDC attached, a design flow consisting of synthesis, place & route and timing verification will illustrate this unique capability
- FPGA emulation of an asynchronous block enabling functional verification of any clockless design

Tiempo's asynchronous technology

The Tiempo solution is centered on its patented clockless design technology, which is offered to customers through fully synthesizable IP blocks. In addition to lower dynamic power consumption, other benefits include:

- Immediate sleep and wake-up
- Lower noise, lower electromagnetic emission
- A wide voltage range
- Higher resistance to PVT variations
- Higher resistance to hardware attacks

Initial implementations of the Tiempo technology have been achieved in low power microcontroller IP cores, as well as cryptoprocessor IP cores for secure applications such as contactless systems. A silicon proof of TAM16 (Tiempo's 16-bit microcontroller core) was implemented in a standard 0.13micron foundry process. The chip showed an impressive 40µA/MIPS. The cryptoprocessor IP family includes all standard ciphering and deciphering algorithms (DES, 3DES, AES as well as an RSA-ECC accelerator).

About Tiempo

Tiempo SAS was founded in 2007 by experienced chip design industry veterans Serge Maginot and Marc Renaudin. Its focus is on developing technology for use in semiconductors requiring low power and/or highly secure operating characteristics. Its patented clockless, delay-insensitive approach to chip design is delivered as highly efficient IP cores that can be implemented using standard EDA tools and formats. Tiempo's solution enables low power design without sacrifices in performance, security or other critical operating requirements impacted by traditional low power design techniques. Tiempo is headquartered near Grenoble, France, with US offices in California. More information can be found at www.tiempo-ic.com.

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