



**Grenoble, France – June 2009** – Tiempo demonstrates the first asynchronous synthesis tool using standard languages at DAC 2009.

Tiempo will reveal at the 46th DAC Conference & Exhibition, July 27-30, 2009, in San Francisco, California, its unique and breakthrough asynchronous synthesis tool. ACC (“Asynchronous Circuit Compiler”) is the first synthesis tool on the market which automatically generates asynchronous and delay-insensitive circuits from a model written in a standard hardware description language.

ACC takes as input a description written in SystemVerilog (IEEE Standard 1800-2005), at TLM level (“Transaction-Level Modeling”), which is perfectly suited for high-level modeling of clockless circuits, and generates as output a gate-level netlist in standard Verilog format. ACC also uses standard cell libraries, which can be augmented by Tiempo with a limited set of specific asynchronous cells for better power/speed/area performances. These unique properties allow ACC to be inserted in any standard design flow.

The use of standard SystemVerilog allows designers to verify asynchronous and mixed asynchronous-synchronous circuits using any industry-standard simulation tools. Predefined asynchronous channels and asynchronous/synchronous interface components, modeled in standard SystemVerilog, as well as a recommended coding style for synthesis, are provided by Tiempo allowing high-level and efficient modeling of asynchronous circuits. The generated Verilog netlist can be placed-and-routed using any standard back-end tool and verified with any static timing analysis and electrical simulation tools.

ACC solves traditional asynchronous methodologies limitations, finally bringing to the designer community the benefits of asynchronous circuits (ultra-low power, ultra-low voltage, etc.) while using a standard design flow. ACC is currently being used by Tiempo engineers for the design of Tiempo asynchronous ultra-low power core IPs, such as microcontroller and crypto-processor cores. As an example, TAM16, Tiempo 16-bit microcontroller core released on November 2008, consumes down to 37  $\mu$ A per MIPS when operating at 0.7 V (47  $\mu$ A at 1.2 V), including leakage current of used CMOS 130 nm general-purpose process. Crypto-processor cores include ultra-low power and secured DES/3DES, AES, RSA and ECC accelerators.

ACC is available to Tiempo IP customers as on optional license attached to any Tiempo core IP license, allowing the customers to independently modify the purchased IPs as well as synthesize customer-specific asynchronous blocks complementing these IPs.

Targeted applications are ultra-low power chips for green electronics or embedded electronics, e.g. power management chips, sensor networks, metering devices, RFID, smartcards, electronics for the automotive, medical devices, and mobiles for consumer markets.

Both ACC design flow and TAM16 chip performances will be demonstrated on Tiempo booth (#4104) at the 46th DAC Conference & Exhibition, July 27-30, 2009, in San Francisco, California.

## **About Tiempo**

Tiempo, located in Montbonnot, France, develops and commercializes Core IPs for the design of innovative integrated circuits that are ultra-low power, ultra-low noise, ultra-low voltage, robust versus PVT variations and secured. TIEMPO IP portfolio includes ultra-low power and secured asynchronous cores of microcontrollers, microprocessors and crypto-processors, and is supported by an automated synthesis tool using standard input language. Targeted core applications are chips for low-power embedded electronics and secured devices.

## **Tiempo**

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