**Tiempo, working with STMicroelectronics, unveils first 32nm clockless test chip**

*Asynchronous circuit demonstrates unprecedented robustness to process variation on 32nm technology, paving the way for first-time-right silicon for advanced process nodes.*

Grenoble, France – May 30, 2012 – Tiempo, a leading provider of innovative clockless technology for the design of advanced integrated circuits, working closely with STMicroelectronics, a global semiconductor leader serving customers across the spectrum of electronic applications and a world leader in advanced processes, today announced the first fully clockless circuit in 32nm. The chip was fabricated as first-time-right silicon, with all chip samples 100% functional.

Designed as a collaboration between the two companies, the test chip demonstrates the unmatched benefits of clockless circuits for advanced process nodes. Using Tiempo's delay-insensitive approach, the test chip, including Tiempo's 16-bit microcontroller (TAM16), was functional through an extended voltage range in all the corners of the process, independent of the wafer position and observed process variability.

The chip was designed using the proven ST 32nm Design Platform, which now includes an asynchronous standard cell library jointly developed with CEA-Leti and Tiempo. "The extreme simplicity of integrating the TAM16 microcontroller on an advanced CMOS process using industry standard EDA tools has proven the robustness of Tiempo's design approach," said Robin Wilson, Technology R&D Design Department Manager at ST, "Furthermore TAM16 operates across a very wide voltage range, without any additional design effort." The test chip was modeled in SystemVerilog and synthesized with Tiempo ACC (Asynchronous Circuit Compiler), then placed-and-routed using standard back-end tools.

As advanced processes are being developed, compensating for process variability is becoming very critical. Designers of traditional clocked circuits have to allow for significant margins to ensure the chip will be functional. "Our clockless approach solves these issues as every chip operates at its optimal speed depending on silicon and manufacturing characteristics," said Serge Maginot, CEO of Tiempo. "We plan to expand to even more advanced nodes and to promote a clockless approach to provide key feedback for technology performance characterization and EDA-vs-silicon correlation."

"ST's collaboration with Tiempo is now yielding valuable 32nm silicon feedback; the results validate our assumptions concerning the application of asynchronous design techniques to enable accurate silicon characterization of advanced CMOS processes," said Philippe Magarshack, Corporate VP, Design Enablement and Services, STMicroelectronics.

Tiempo will be demonstrating its asynchronous technology and design flow at the Design Automation Conference, San Francisco, June 4-6$^{th}$, 2012, booth #1001.

**About Tiempo**
Tiempo offers unique chip solutions and EDA tools for advanced ICs. Tiempo solution relies on an innovative and patented clockless design technology using standard hardware description languages and ACC, its unique automated synthesis tool for clockless and delay-insensitive designs. Tiempo is headquartered near Grenoble, France, with US offices in California. More information can be found at www.tiempo-ic.com.

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