TPKA: Asynchronous public key accelerator IP

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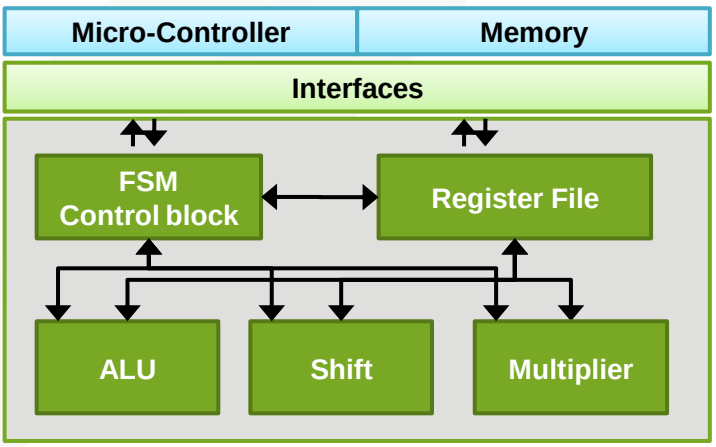
Tiempo clockless crypto-processor core - TPKA - is a public key encryption and decryption accelerator. It is able to execute the standard RSA encryption and decryption algorithms. It can also be used as an accelerator for ECC computations. This IP is designed in Tiempo fully asynchronous and delay insensitive technology that allows ultra-low power consumption, ultra-low noise, ultra-low EMI, as well as robustness against attacks by power analysis & fault injection.

Applications

Targeted applications are chips for smart cards (with or without contact), RFID tags, sensor networks, systems embedding NFC technology and other secured applications

TPKA Block Diagram



Key benefits

- Ultra low power consumption: low energy, low current peaks
- Ultra low electromagnetic emission (EMI/EMC)
- High speed under low/variable power (independently from system clock)
- High robustness against any PVT (process, voltage, temperature) variation
- High robustness against attacks by power analysis and fault injections (for secured applications)

Key features

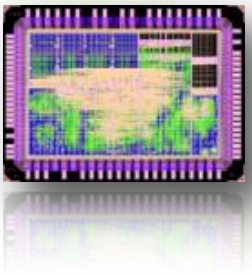
- Executes RSA standard encryption and decryption algorithms
  - Data and key: up to 2048 bits
- ECC – GF(p) – encryption and decryption algorithms primitives available
- Fully asynchronous (no clock) and delay insensitive (correctness of encryption / decryption is guaranteed regardless of any actual delay in internal gates and wires
- Available as Verilog netlist ready for P&R (silicon-proven netlist) or as a GDSII hard-IP block (verified layout description) [1]
- Option: IP *secured* against attacks by power analysis and fault injection

[1] Please contact Tiempo for available libraries and technologies

Supported operations

A xor B (bitwise exclusive or)	$A / 2^I$ (right shift)
A and B (bitwise and)	A*B (multiplication)
A + B (addition)	$A*B*2^{-n}$ mod M (Montgomery multiplication)
A - B (subtraction)	A^K mod M (exponentiation)
R =A (copy)	A^K mod M (sliding windows)
$A*2^I$ (left shift)	A^K mod M (exponentiation with Montgomery ladder)

Tiempo TESIC chip



Silicon Proven

Designed and processed on TSMC CMOS 130 nm LP technology.

Characteristics

Figures below are electrical measurements made on Tiempo prototype chip TESIC fabricated on a TSCM130LP 1.5V process. Figures are valid for the *secured* version of the IP.
These figures illustrate one instance of the IP and can be tuned to our customer needs (reduced power consumption or increased performance).

Supply voltage	1.0V	1.5V
RSA CRT 1024 speed (ms)	46.5	18.4
Average current (mA)	2.00	7.62
Energy (µJ)	94	215

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