Asynchronous TAM16 Core IP

Targeted applications are ultra-low power chips for embedded electronics, e.g. power management chips, sensor networks, metering devices, RFID, smartcards, but also chips that must operate with low electromagnetic emissions, e.g. electronics for the automotive and the medical industries.

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Key benefits

• Ultra low power consumption: low energy (divide by 4 to 5), low current peaks (divided by 10 to 15)
• Ultra low noise, ultra low electromagnetic emission (EMI/EMC)
• Easy-programmable, fast and energy-efficient interrupt management & peripheral communications
• Fast wake-up time (< 5 ns), immediate sleep-mode
• High robustness against any PVT (process, voltage, temperature) variation
• High robustness against attacks by power analysis and fault injections (for secured applications)
Key features

- 16-bit microcontroller core with power-efficient instruction set,
- Software development kit (with assembler, linker, instruction set simulator and debugger),
- Embedded peripherals including:
  - 1 UART
  - 3 Cascadable Timers
  - Interrupt Controller for vectorized interrupt handling
  - 16-bit Programmable Input/Output (PIO)
  - Boot pins for boot configurations
- Two memory interfaces:
  - An interface for third-party standard ROM and RAM, with memory redundancy module to replace faulty RAM pages
  - An interface for the peripheral memory space, allowing for synchronized and nonsynchronized communications
- Fully asynchronous (no clock) and delay insensitive (functional correctness guaranteed regardless of any actual delay in internal gates and wires)
- Available as Verilog netlist ready for P&R (silicon-proven netlist)
- As an option: Verilog netlist secured against attacks by power analysis and fault injection
- As an option: Verilog netlist strengthened for ultra low noise, ultra low EMI

For more information, please contact Tiempo at:

www.tiempo-ic.com

Silicon-proven

Designed and processed in a general-purpose CMOS 130 nm technology, Tiempo TAM16 chip instantiates TAM16 Core IP and third-party 16 KB RAM and 1 KB ROM (that includes a 412-instruction BIST).

This chip was fully operational at first run and with expected power performances:
- ultra-low power consumption: < 40 μA per MIPS
- low voltage: 0.7 V

1 Please contact Tiempo for available libraries and technologies